APPENDIX C
complete set of "clean" claims
pursuant to 37 C.F.R. §1.121(c)(3)

9. The process of manufacture of a MOSgated device comprising:

forming a gate oxide layer atop a silicon surface of one conductivity type;

forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and said underlying gate oxide layer into a plurality of stripes of oxide and polysilicon spaced 1 to 4 microns and overlying said oxide; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of polysilicon as a mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; diffusing second base diffusion stripes, into said silicon surface, using said stripes of polysilicon as a mask, to a depth below that of said source diffusions and a width substantially equal to the space between the opposite edges of adjacent pairs of said polysilicon stripes.

10. The process of claim 9, wherein said polysilicon stripes have a width of about 3.1 microns and a spacing of about 1.25 microns.

11. The process of claim 9 wherein said first base diffusions have a depth of about 1.25 microns and said source diffusions have a depth of about 0.4 microns.

12. The process of claim 10 wherein said first base diffusions have a depth of about 1.25 microns and said source diffusions have a depth of about 0.4 microns.

13. The process of claim 9 which further includes the formation of insulation spacer layers over the type and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

14. The process of claim 12 which further includes the formation of insulation spacer layers over the type and edges of said polysilicon stripes and the etching of shallow openings through central

portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

15. The process of claim 9 wherein said first base diffusions and said second base diffusions are formed at substantially the same depth.

16. The process of claim 9 wherein said polysilicon stripes are spaced 1.5 microns apart.

17. The process of claim 9 wherein said polysilicon stripes are spaced 3.2 to 3.4 microns wide.